REMARKS

At the outset, Applicant expresses appreciation to the Examiner for pointing out the informalities in the claims. Amendments have been made and the rejection under 35 U.S.C. § 112, second paragraph, have been obviated. Entry of the amendments and withdrawal of the rejections is respectfully requested.

Claims 1, 7 and 14 have been rejected under 35 U,S,C, § 103(a) as being unpatentable over Biemond in further view of Nash. Reconsideration is respectfully urged.

In order for a finding of obviousness, according to MPEP § 2142, a proper prima facie case of obviousness can be established only when all three basic criteria are met. These are: (1) some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the references or to combine the reference teachings; (2) there must be a reasonable expectation of success; and (3) the combination of references must teach or suggest all the claim limitations. These must not be based on applicants' disclosure.

Biemond is cited as disclosing an iterative method for image deblurring using a computer. The Examiner has taken official notice that it is "notoriously well known" to download images for processing. Similarly there is no disclosure of uploading the deblurred image. Biemond does not disclose logic blocks and certainly does not suggest sequential exchange of data between interconnected adjacent processing logic blocks. On page 860 of this reference, Fig. 7 discloses that the point spread function is weighted by the fraction of the pixel covered. There is no disclosure that groups of pixels arrive in processing logic blocks.

Nash is cited for teaching that the systolic array is broken into processing elements (the language of Nash) which the Examiner then equates as processing logic blocks. However there is no suggestion in Nash (or the other references) that processing elements are processing logic blocks as called for by the instant claims. Further, the Examiner has taken the phrase "image restoration" that is briefly noted in Nash to imply that Nash is adaptable to do deblurring. That is not disclosed. More importantly, Nash is concerned with a linear systolic array. It is not capable of performing computations that "are, however, performed in parallel by the processing logic blocks of the array." (Page 11, lines13-14 of this application as filed). The independent claims have been amended to more clearly describe this parallel calculation.

The Examiner also notes that Owens teaches the use of systolic algorithms, but has not cited that reference in this rejection. Still, Owen does not remedy the deficiencies of this rejection. There is no motivation to modify the references to use parallel calculations with adjacent processing logic blocks, and thus the combination of Biemond with Nash and Owen does not meet the first criteria or MPEP § 2142. Withdrawal of the rejection is earnestly solicited.

Claims 5, 12 and 19 have been rejected under 35 U,S,C, § 103(a) as being unpatentable over Biemond in view of Nash, in further view of Owen. The Examiner concedes that Biemond and Nash do not discuss how the pixels are grouped for processing, and has cited Owen to show that a single pixel is operated on per processor. While that may be true, it does not remedy the deficiency of the primary references that do not disclose parallel calculations with adjacent processing logic blocks. Withdrawal of the rejection is respectfully urged.

Claims 2, 8 and 15 have been rejected under 35 U,S,C, § 103(a) as being unpatentable over Biemond in view of Nash, in further view of Jagadish. This last reference is cited as teaching the "implementation of iterative algorithms on a processing array." Once again the combination does not disclose or suggest parallel calculations with adjacent processing logic blocks. Withdrawal of the rejection is requested.

Claims 3-4, 9-11 and 16-18 have been rejected under 35 U,S,C, § 103(a) as being unpatentable over Biemond in view of Nash and Jagadish, in further view of Gorinevsky. This latter reference relates to mathematical calculations but in no way looks at image deblurring and has been cited based only on Applicant's disclosure and not in accordance with MPEP § 2142. The Examiner has made reference to Dowski (US 2003/169944) but that reference was not listed on the Notice of References cited. Nevertheless, Dowski does not remedy the deficiencies of the other references simply by dividing an image into color spaces and does not teach deblurring. "Further processing" does not teach deblurring. Withdrawal of the rejection is urged.

Claims 6, 13 and 20 have been rejected under 35 U,S,C, § 103(a) as being unpatentable over Nash in view of Owen. As has been demonstrated above, Nash does not teach parallel calculations and Owen does not remedy that deficiency.

In summary, it is respectfully submitted that a prima facie case of obviousness has not been made by the cited references. Reconsideration of the rejections is respectfully requested and allowance of the claims is earnestly solicited.

DATE: August 2, 2007

Respectfully submitted,
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CERTIFICATE OF MAILING

I hereby certify that the attached correspondence is being deposited with the United States Postal Service and First Class Mail in an envelope addressed to: Mail Stop non fee amendment, Commissioner for Patents, PO Box 1450, Alexandria, VA, 22313-1450, on the date appearing below.

DATE: August 2, 2007

Respectfully submitted,

John S. Munday